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| 10/563,298 | 01/03/2006 | Yoshitoshi Kida | SON-3057 | 1328 |

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| EXAMINER | |
|---|---|
| WILLIS, RANDAL L | |

| ART UNIT | PAPER NUMBER |
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| 2629 | |

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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/563,298 | KIDA ET AL. | |
| | Examiner | Art Unit | |
| | RANDAL WILLIS | 2629 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *03 January 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6 and 7* is/are rejected.

7)☒ Claim(s) *5* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 January 2006* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *1/3/06, 9/17/08, 12/12/08*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

1. This office action is in response to application 10/563298 filed January 3rd 2006. Claims 1-7 are currently pending and have been examined.

### *Priority*

2. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

### *Information Disclosure Statement*

3. The information disclosure statements (IDS) submitted on 12/12/2008, 9/17/2008 and 1/03/2006 are in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statements are being considered by the examiner.

### *Drawings*

4. Figures 1 and 2 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled “Replacement Sheet” in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted

by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

### *Claim Rejections - 35 USC § 102*

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1, 3-4, 6-7 rejected under 35 U.S.C. 102(b) as being anticipated by Matsukuma (EP 1083540).

Apropos claim 1, Matsukuma teaches:

A flat display apparatus in which a display unit formed by arranging pixels in a matrix and a drive circuit driving the display unit are formed integrally on a substrate (Fig. 4), characterized in that:

the drive circuit has a first circuit block operating by a first power supply voltage (Booster circuit 7 and power supply selector 1, Fig. 4) and a second circuit block operating by a second power supply voltage (segment driver 3, shown in Fig. 5 to receive power supply VSL which is less than VLC0), which is lower than the first power supply voltage, for processing a processing result by the first circuit block;

the second circuit block receives an input of one processing result of the first circuit block at an active element performing on-off operation complementarily (The transistors 30 and 31 receive the processed result of VSL from 1, Fig. 5); and

the first circuit block has a level setting circuit for setting a level of the one processing result so as to hold an output of the active element at a predetermined level by a fall of the first power supply voltage ([0059] and [0060]).

Apropos claim 3, Matsukuma teaches:

The flat display apparatus according to claim 1, characterized in that:

the second circuit block is a drive circuit for switching electrode potential of a storage capacitor provided in each of the pixels (3 is a driver for the pixels of an LCD panel, which inherently have storage capacitors [0057] and [0059]); and

the active element performing on-off operation complementarily is an active element for outputting the output to the storage capacitor to switch the electrode potential according to the one processing result (transistors in 3 switch the pixels to ground or VSL [0059]).

Apropos claim 4, Matsukuma teashes:

The flat display apparatus according to claim 1, characterized in that:

the second circuit block is a drive circuit for switching electrode potential of liquid crystal cells of the pixels (Panel 9 is LCD [0059]); and

the active element performing on-off operation complementarily is an active element for outputting the output to the liquid crystal cells to switch the electrode potential according to the one processing result (transistors in 3 switch the pixels to VCH or VCL, where VSL is determined to be ground or VLC2 based on the processed result [0059]).

Apropos claim 6, Matsukuma teaches:

The flat display apparatus according to claim 1, characterized by comprising:

a power supply circuit for generating a power supply by the first power supply voltage (Boosting circuit 7, Fig. 4) from a power supply by the second power supply voltage, wherein

the power supply by the second power supply voltage is supplied externally (Voltage comes from 72, Fig. 4).

Apropos claim 7, Matsukuma teaches:

An integrated circuit having a first circuit block operating by a first power supply voltage (Booster circuit 7 and power supply selector 1, Fig. 4) and a second circuit block operating by a second power supply voltage, which is lower than the first power supply voltage(segment driver 3, shown in Fig. 5 to receive power supply VSL which is less than VLC0), for processing a processing result by the first circuit block , characterized in that:

the second circuit block receives an input of one processing result of the first circuit block at an active element performing on-off operation complementarily(The transistors 30 and 31 receive the processed result of VSL from 1, Fig. 5); and

the first circuit block has a level setting circuit for setting a level of the one processing result so as to hold an output of the active element at a predetermined level by a fall of the first power supply voltage([0059] and [0060]).

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claim 2 rejected under 35 U.S.C. 103(a) as being unpatentable over Matsukuma in view of Nakajima (20030011548).

Apropos claim 2, Matsukuma fails to explicitly teach:

the active element performing on-off operation complementarily is an active element of a switch circuit for switching a polarity of the generated reference voltage by outputting the output to the resistance block to switch a terminal voltage of the resistance block according to the one processing result.

the second circuit block is a reference voltage generating circuit for generating a plurality of reference voltages by resistively dividing a reference voltage by a resistance block, and a reference voltage selector for selectively outputting the plurality of reference voltages according to gradation data showing gradation of the pixels; and

In the same field of LCD displays, Nakajima teaches having a DAC circuit in the driver of the display device that resistively divides a voltage and selectively supplies the voltage to the pixels of the display (See Fig. 7, the on/off complementary switches SW1-SW4 reverse the polarity of the voltages for the display panel).

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to replace the data driver of Matsukuma with the reference voltage generator as taught by Nakajima in order to reduce power consumption ([0010]) and drive the display with different grayscale voltages.

### ***Allowable Subject Matter***

Claim 5 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

## *Conclusion*

Any inquiry concerning this communication or earlier communications from the examiner should be directed to RANDAL WILLIS whose telephone number is (571)270-1461. The examiner can normally be reached on Monday to Thursday, 8am to 5pm (EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on 571-272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

RLW

Amr Awad/
Supervisory Patent Examiner, Art Unit 2629